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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,603	08/20/2003	Kazuyuki Yamada	9319S-000540	5576
27572	7590	05/05/2006	EXAMINER	
HARNESS, DICKY & PIERCE, P.L.C. P.O. BOX 828 BLOOMFIELD HILLS, MI 48303			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	
DATE MAILED: 05/05/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/644,603

Applicant(s)

YAMADA ET AL.

Examiner

Alexander O. Williams

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9 and 24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9 and 24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/28/06.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Art Unit: 2826

Serial Number: 10/644603 Attorney's Docket #: 9319S-000540
Filing Date: 8/20/2003; claimed foreign priority to 7/15/2003 and 8/21/2002

Applicant: Yamada et al.

Examiner: Alexander Williams

Applicant's RCE/Amendment filed 2/20/06 to the election with traverse of Species I of figure 3 (claims 9-15) filed 1/21/05 is acknowledged.

Claims 1-8 and 10-23 have been cancelled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Gurtler et al.
(U.S. Patent # 5,457,879).

9. Gurtler et al. (figures 1 to 11) specifically figure 1 show a semiconductor device mounting structure including a semiconductor device **24** having an electrode **36** and a substrate **12** having a wiring terminal **22** that is conductively connected to

the electrode, wherein a width of the wiring terminal is smaller than a width of the electrode; a recessed portion (**within 36**) formed in a center portion of the electrode **36** before the electrode and the wiring terminal are conductively connected, the recessed portion is constituted by a dimension corresponding to the width of the wiring terminal; and the one of the electrode and the wiring terminal is embedded in a surface of the other of the electrode and the wiring terminal.

Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by Hedler (U.S. Patent # 6,555,415 B2).

9. Hedler (figures 1 to 24) specifically figure 18 show a semiconductor device mounting structure including a semiconductor device **9** having an electrode **8a** and a substrate **109** having a wiring terminal **103a-f** that is conductively connected to the electrode, wherein a width of the wiring terminal is smaller than a width of the electrode; a recessed portion (**within 8a**) formed in a center portion of the electrode **8a** before the electrode and the wiring terminal are conductively connected, the recessed portion is constituted by a dimension corresponding to the width of the wiring terminal; and the one of the electrode and the wiring

terminal is embedded in a surface of the other of the electrode and the wiring terminal.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, and with respect to claims 9 and 24, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Hatakeyama Tomoyuki (Japan Patent # 11-251363).

9. Tomoyuki (figures 1 to 13) specifically figures 1 and 2 show a semiconductor device mounting structure including a semiconductor device **1** having an electrode **3** and a substrate **5** having a wiring terminal **4** that is conductively connected to the electrode, wherein a width of the wiring terminal is smaller (**this portion of the 4 width being at the intersection of the bottom of 3**) than a width of the electrode (**this width being at the bottom of 3**); a recessed portion (**4b being the center recessed portion of 3 in which 4 fills**) formed in a center portion of the electrode **3**, the recessed portion (**4b being the center recessed portion of 3 in which 4 fills**) is constituted by a dimension corresponding to the width of the wiring terminal (**outer lining of 4 with in 3**); and the one of the electrode and the wiring terminal is embedded in a surface of the other of the electrode and the wiring terminal. Applicant's claim language of a recessed portion formed in a center portion of the electrode before the electrode and the wiring terminal are conductively connected is given little weight. In a device claim, the Examiner is interested in finding the final structure claimed by Applicant. Whether the recess portion formed in a center portion of the electrode was created before or after the conductive connection to the wiring terminal, the same final structure occurs if a recess is present in the structure (**clearly shown in figure 4**).

As to the grounds of rejection under section 103, see MPEP § 2113.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima Yohei (Japan Patent # 2001-223243).

9. Yohei (figures 1 to 12) specifically figure 1(B) show a semiconductor device mounting structure including a semiconductor device **10** having an electrode **16** and a substrate **20** having a wiring terminal **22** that is conductively connected to

the electrode **22**, wherein a width **(from one end of 22 to the other end)** of the wiring terminal is smaller than a width of the electrode **(from one end of 16 to the other end)**; a recessed portion **(at 27 is where a whole is within 16 and where 22 fill the recessed portion)** formed in a center portion of the electrode, the recessed portion is constituted by a dimension corresponding to the width of the wiring terminal; and the one of the electrode and the wiring terminal is embedded in a surface of the other of the electrode and the wiring terminal. Applicant's claim language of a recessed portion formed in a center portion of the electrode before the electrode and the wiring terminal are conductively connected is given little weight. In a device claim, the Examiner is interested in finding the final structure claimed by Applicant. Whether the recess portion formed in a center portion of the electrode was created before or after the conductive connection to the wiring terminal, the same final structure occurs if a recess is present in the structure.

As to the grounds of rejection under section 103, see MPEP § 2113.

Claim 24 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Gurtler et al. (U.S. Patent # 5,457,879) in view of Applicant's Prior Art figures 10 and 11.

24. Gurtler et al. (figures 1 to 11) specifically figure 1 show a device comprising: a retaining substance **36**; a wiring substrate **12** including a wiring terminal **22** conductively connected; and a semiconductor device **24** including an electrode **36** conductively connected to the wiring terminal; wherein: a width of the wiring terminal is smaller than a width of the electrode; a recessed portion formed in a center portion of the electrode before the electrode and the wiring terminal are conductively connected, the recessed portion is constituted by a dimension corresponding to

the width of the wiring terminal; and the wiring terminal is embedded in a surface of the electrode. Gurtler et al. fail to explicitly show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance.

Applicant's Prior Art figures 10 and 11 disclose show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Therefore, it would have been obvious to one of ordinary skill in the art to the teach of Applicant's Prior Art figures 10 and 11 to modify Gurtler et al.'s device for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Claim 24 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hedler (U.S. Patent # 6,555,415 B2) in view of Applicant's Prior Art figures 10 and 11.

24. Hedler (figures 1 to 24) specifically figure 18 show a device comprising: a retaining substance **8a**; a wiring substrate **109** including a wiring terminal **103a-f** conductively connected; and a semiconductor device **9** including an electrode **8a** conductively connected to the wiring terminal; wherein: a width of the wiring terminal is smaller than a width of the electrode; a recessed portion formed in a center portion of the electrode before the electrode and the wiring terminal are conductively connected, the recessed portion is constituted by a dimension corresponding to the width of the wiring terminal; and the wiring terminal is embedded in a surface of the electrode. Hedler fail to explicitly

show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance.

Applicant's Prior Art figures 10 and 11 discloses show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Therefore, it would have been obvious to one of ordinary skill in the art to the teach of Applicant's Prior Art figures 10 and 11 to modify Hedler's device for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Claim 24 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatakeyama Tomoyuki (Japan Patent # 11-251363) in view of Applicant's Prior Art figures 10 and 11.

24. Tomoyuki (figures 1 to 13) specifically figures 1 and 2 show a device comprising: a retaining substance **6**; a wiring substrate **10** including a wiring terminal **4** conductively connected; and a semiconductor device **1** including an electrode **3** conductively connected to the wiring terminal; wherein: a width of the wiring terminal is smaller than a width of the electrode; a recessed portion formed in a center portion of the electrode, the recessed portion is constituted by a dimension corresponding to the width of the wiring terminal; and the wiring terminal is embedded in a surface of the electrode. Applicant's claim language of a recessed portion formed in a center portion of the electrode before the electrode and the wiring terminal are conductively connected is given little weight. In a device claim, the Examiner is interested in finding the final structure claimed by Applicant. Whether the recess portion formed in a center portion of the

electrode was created before or after the conductive connection to the wiring terminal, the same final structure occurs if a recess is present in the structure. Tomoyuki fail to explicitly show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance.

Applicant's Prior Art figures 10 and 11 discloses show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Therefore, it would have been obvious to one of ordinary skill in the art to the teach of Applicant's Prior Art figures 10 and 11 to modify Tomoyuki's device for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

As to the grounds of rejection under section 103, see MPEP § 2113.

Claim 24 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurashima Yohei (Japan Patent # 2001-223243) in view of Applicant's Prior Art figures 10 and 11.

24. Yohei (figures 1 to 12) specifically figure 3 show a device comprising: a retaining substance **27**; a wiring substrate **20** including a wiring terminal **22** conductively connected; and a semiconductor device **10** including an electrode **16** conductively connected to the wiring terminal; wherein: a width of the wiring terminal is smaller than a width of the electrode; and the wiring terminal is embedded in a surface of the electrode; a recessed portion formed in a center portion of the electrode, the recessed portion is constituted by a dimension corresponding to the width of the wiring terminal; and the wiring terminal is embedded in a

surface of the electrode. Applicant's claim language of a recessed portion formed in a center portion of the electrode before the electrode and the wiring terminal are conductively connected is given little weight. In a device claim, the Examiner is interested in finding the final structure claimed by Applicant. Whether the recess portion formed in a center portion of the electrode was created before or after the conductive connection to the wiring terminal, the same final structure occurs if a recess is present in the structure. Yohei fail to explicitly show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance.

Applicant's Prior Art figures 10 and 11 discloses show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Therefore, it would have been obvious to one of ordinary skill in the art to the teach of Applicant's Prior Art figures 10 and 11 to modify Yohei's device for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

As to the grounds of rejection under section 103, see MPEP § 2113.

Response

Applicant's arguments filed 2/20/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Art Unit: 2826

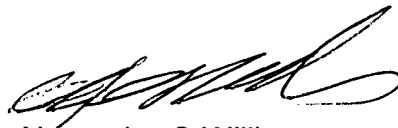
Field of Search	Date
U.S. Class and subclass: 257/778,738,738,777,780,784,786,734,787,728,787,780, 29/837,740	4/17/05 9/15/05 4/30/06
Other Documentation: foreign patents and literature in 257/778,738,738,777,780,784,786,734,787,728,787,780, 29/837,740	4/17/05 9/15/05 4/30/06
Electronic data base(s): U.S. Patents EAST	4/17/05 9/15/05 4/30/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2826

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
4/30/06